REMARKS

Reconsideration and withdrawal of the rejections set forth in the Office Action dated May 5, 2004 are respectfully requested. Claims 1-30 remain pending. In the outstanding Office Action claims 1-18 were indicated allowable, claims 19-23,26 and 28-30 were rejected, and claims 24-25 and 27 were objected to. A separate petition for a 1-month extension of time accompanies this amendment.

The Examiner is thanked for the helpful telephone interview with the undersigned Agent on June 22, 2004. The agreement reached during the interview is reflected in the remarks and amendments herein. Claims 19-22 have been amended accordingly.

Rejections under 35 U.S.C. § 102

Claims 19-23, 26 and 28-30 have been rejected as being anticipated by Testin, US Patent No. 5,376,928.

As discussed in the interview, the present invention relates to embedding clock and data signals within high-speed bus lines. Specific features of the instant invention include mapping schemes used to transmit both clock and data signals on one given data line within the parallel bus. See for example, Figures 2-4 and pages 3-5 of the specification which describe how a multiplexer changes the data signals (D) and clock information (1 or 0) using 9 parallel bit lines (B). These tables further detail how the bit/data information changes for each specific time period during transmission.

As also discussed during the telephone interview, the patent to Testin shows a signal processing system with multiple busses. The protocols on these busses may be changed due to electrical interference from one bus to another. The difference between Testin and the present invention is that the busses in the Testin reference are serial busses, while the instant invention employs parallel busses.

Claims 19-22 have been amended herein to recite the feature that the "multiplexer maps the data bits and clock bit onto a corresponding number of different parallel bus lines at different time periods". This clearly defines the present invention over the Testin device, wherein each bus in Testin is a serial bus that consists of one wire. The claimed invention is therefore not taught nor rendered obvious by Testin or any of the other cited references.

It was also discussed and agreed during the telephone interview, that claim 23 as originally filed in fact does define over the Testin reference. The recitation of "..."B" data lines wherein the number "B" equals "D" plus one...", essentially defines a parallel bus, a feature not taught by Testin.

Conclusion

In view of the foregoing, claims 1-30 comply with the requirements of 35 U.S.C. § 112 and patentably define over the cited art. A Notice of Allowance is, therefore, respectfully requested. If the Examiner has any questions or believes another telephone conference would further expedite prosecution of this application, the Examiner is encouraged to call the undersigned Agent at (202) 434-1630.

Respectfully submitted,
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Date: August 11, 2004

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